DECLARATION

I, the undersigned, Keiji HABA of c/o ARCO PATENT OFFICE at 3rd Fl., Bo-eki Building, 123-1 Higashi-machi, Chuo-ku, Kobe-shi 650-0031 JAPAN, hereby declare that I am conversant with Japanese and English languages and that attached is, to the best of my knowledge and belief, a true translation of the Japanese Patent Application No. JP 2002-011833 filed on January 21, 2002.

Dated this 28th day of April, 2005

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PATENT OFFICE
JAPANESE GOVERNMENT

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Date of Application: January 21, 2002

Application Number: JP2002-011833

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Certified on January 7, 2003
By Shinichiro OHTA, Commissioner, Patent Office

Number of certification: 2002-3104027

【Name of Document】 Patent application.

【Reference Number】 2030230057

【Date of Submission】 January 21, 2002

【Address】 Commissioner, Patent Office

【International Patent Classification】 H01L 29/78
H01L 29/778

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【Indication of Charge】
【Prepayment Register Number】 014409
【Amount Prepaid】 21,000 yen.

【List of Documents Submitted】
【Name of Document】 Specification 1 copy
【Name of Document】 Drawing 1 copy
【Name of Document】 Summary 1 copy
【General Power of Attorney Number】 0006010

【Whether Proof Is Needed or Not】 Needed

Number of certification: 2002-3104027

[Name of the Document] SPECIFICATION

[Title of the Invention] SEMICONDUCTOR DEVICE

[Claims]

[Claim 1] A semiconductor device comprising:

a semiconductor layer;

a gate insulator provided on the semiconductor layer;

a gate electrode provided on the gate insulator;

a source region and a drain region, which are of a first conductivity type and are provided in the semiconductor layer on both sides of the gate electrode;

a channel region comprising a first semiconductor which is provided in a region in the semiconductor layer which is positioned between the source region and the drain region; and

an under-channel region that is provided immediately under the channel region and that comprises a second semiconductor having a band gap larger than that of the first semiconductor; and

a voltage application means for applying, to the under-channel region, a bias in a direction in which the threshold value voltage becomes higher in the stand-by state than in an operation state.

[Claim 2] The semiconductor device according to claim 1, characterized in that:

the semiconductor device further comprises a cap layer comprising a third semiconductor that is provided between the channel region and the gate insulator in the semiconductor layer and that has a band gap larger than that of the first semiconductor.

[Claim 3] The semiconductor device according to claim 1 or 2, characterized in that:

the first semiconductor is a semiconductor having a composition represented by $Si_{1-x-y}Ge_xC_y$ ($0 \leqq x < 1$, $0 \leqq y < 1$); and

the second semiconductor is Si.

[Claim 4] The semiconductor device according to claim 2, characterized in that:

the first semiconductor is a semiconductor having a composition represented by $Si_{1-x-y}Ge_xC_y$ ($0 \leqq x < 1$, $0 \leqq y < 1$); and

the cap layer is made of Si.

[Claim 5] The semiconductor device according to any one of claims 1 to 4, characterized in that;

an insulating layer is provided under the semiconductor layer.

[Claim 6] The semiconductor device according to any one of claims 1 to 5, characterized in that:

the source region and the drain region are p-type source region and p-type drain region, respectively; and

the channel region is a channel region for a p channel.

[Claim 7] The semiconductor device according to claim 6, characterized in that:

the first semiconductor is a semiconductor comprising Si and Ge as components; and

the p channel is a buried channel.

[Claim 8] The semiconductor device according to any one of claims 1 to 5, characterized in that:

the source region and the drain region are a n-type source region and the n-type drain region; and

the channel region is a channel region for a n channel.

[Claim 9] The semiconductor device according to claim 8, characterized in that:

the first semiconductor is a semiconductor comprising Si and C as components; and

the n channel is a buried channel.

[Claim 10] The semiconductor device according to claim 8, characterized in that:

the first semiconductor is a semiconductor having a composition represented by $Si_{1-x-y}Ge_xC_y$ ($0 \leqq x < 1$, $0 \leqq y < 1$); and

the under-channel region is doped with boron.

[Claim 11] The semiconductor device according to claim 6, characterized in that:

the semiconductor device further comprises:

another one semiconductor layer provided on the substrate;

another one gate insulator provided on the another one semiconductor

layer;

another one gate electrode provided on the another one gate insulator;

an n-type source region and an n-type drain region provided at both sides of the another one gate electrode in the another one semiconductor layer;

a channel region for n channel comprising the first semiconductor which is provided in a region in the another one semiconductor layer which is positioned between the n type source region and the n type drain region; and

another one under-channel region that is provided under the channel region for n channel and that comprises the second semiconductor; and

another one voltage application means for applying, to the another one under-channel region, a bias in a direction in which the threshold value voltage becomes higher in the stand-by state than in an operation state; and

wherein the semiconductor device functions as a complementary semiconductor device.

[Claim 12] The semiconductor device according to claim 11, characterized in that:

the first semiconductor is a semiconductor comprising Si and Ge as components; and

the p channel is a buried channel.

[Claim 13] The semiconductor device according to claim 12, characterized in that:

the first semiconductor is a semiconductor comprising Si, Ge, and C as components; and

the p channel and the n channel are both buried channels.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a semiconductor device comprising a heterojunction type MIS transistor and, more particularly, to a measure for maintaining the operation speed while reducing the voltage.

[0002]

[Prior Art]

In recent years, battery-operated personal digital assistant apparatus has

been widely used. It is strongly desired that such an apparatus operates at a reduced power supply voltage while keeping high-speed operation performance in order to extend the life of the battery used.

[0003]

The power consumption (**Pload**) of a circuit comprising a complementary MIS device (cMIS device), which is caused predominantly by charge-discharge of load, is represented by the following expression (1):

$$\mathbf{Pload} = f \cdot \mathbf{Cload} \cdot \mathbf{VDD}^2 \qquad \ldots(1)$$

wherein f is an operation frequency of load, **Cload** is a load capacitance, and **VDD** is a power supply voltage. As can be understood from the formula (1), reducing the power supply voltage **VDD** is very effective in reducing the power consumption. However, the operation speed of MIS transistors, in general, also lowers with lowering power supply voltage. It is therefore desired that the power supply voltage of a MIS transistor be reduced and, at the same time, the high-speed operation performance of the MIS transistor be maintained as it is.

[0004]

Although lowering of the threshold voltage of a MIS transistor is effective in realizing a high-speed operation (i.e., a high driving power) with a high on-current being ensured at a low power supply voltage, generally the subthreshold leakage current increases exponentially with lowering threshold voltage. In a circuit comprising a cMIS device, power consumption based on charge-discharge of load does not occur in a stand-by state and, hence, the proportion of power consumption based on the subthreshold leakage current to the power consumption of the chip increases. As the art of reducing such a subthreshold leakage current in the stand-by state, there is known a VTMIS device (Variable Threshold-Voltage MIS device) of which the threshold voltage is controlled by varying the substrate bias, as taught by literature document 1 (T. Kuroda et. Al., "A 0.9V, 150-MHz, 10-mW, 4mm2, 2-D Discrete Cosine Transform Core Processor with Variable Threshold-Voltage(VT) Scheme," IEEE J. Solid-State Circuits, vol.31, 1996, p.1770.), for example. When the VTMIS device is in its operating state, a high-speed operation is ensured in the device by applying a reduced substrate bias to lower the threshold voltage of the MIS transistor, whereas when the device is in its stand-by state, the leakage current is reduced in the device by applying an enhanced substrate bias to raise the threshold voltage of the MIS

transistor.

[0005]

[Problems to be Solved by the Invention]

Such a VTMIS device, however, involves the following problem.

[0006]

In order for a MIS transistor to realize a high-speed operation in its operating state as well as a low leakage current in its stand-by state, the threshold voltage of the MIS transistor has to shift largely with varying substrate bias. As the power supply voltage will be lowered more and more from now on, it will be difficult to obtain a large shift in the threshold voltage of the MIS transistor. A change in threshold voltage (ΔVth) due to a change in substrate bias (ΔVbs) is represented by the following expression (2):

$$\Delta Vth = \gamma \cdot \Delta Vbs \quad \ldots(2)$$

wherein γ is a substrate bias coefficient.

[0007]

Since a reduction in threshold voltage Vth and an improvement in substrate bias coefficient γ are in a tradeoff relation to each other as taught by literature document 2 (T. Hiramoto et. Al., "Low Power and Low Voltage MOSFETs with Variable Threshold Voltage Controlled by Back-Bias," IEICE Trans. Electron., vol.E83-C, 2000, p.161), a MIS transistor having a low threshold voltage has decreased substrate bias coefficient γ undesirably. Therefore, if the threshold voltage Vth of the MIS transistor in the operating state is lowered to lower the power supply voltage of the transistor as well as to realize a high-speed operation (i.e., a high driving power), the substrate bias coefficient γ decreases accordingly and, hence, the amount of change ΔVth in threshold voltage Vth decreases, as can be understood from the expression (2). That is, even if the MIS transistor is applied with a strong substrate bias in the stand-by state, the amount of change ΔVth from the threshold voltage Vth of the transistor in the operating state to that of the transistor in the stand-by state is not made large enough. As a result, it might be difficult to suppress the subthreshold leakage current of the MIS transistor sufficiently.

[0008]

It is an object of the present invention to provide a semiconductor device which is capable of realizing a low off-leakage current while ensuring a high-speed

operation for a MIS transistor by employing means for ensuring a sufficiently large substrate bias coefficient γ while lowering the threshold voltage of the MIS transistor.

[0009]

[Means for Solving the Problem]

The semiconductor device of the present invention comprises: a semiconductor layer; a gate insulator provided on the semiconductor layer; a gate electrode provided on the gate insulator; a source region and a drain regions, which are of a first conductivity type and are provided in the semiconductor layer on both sides of the gate electrode; a channel region comprising a first semiconductor which is provided in a region in the semiconductor layer which is positioned between the source region and the drain region; and an under-channel region that is provided immediately under the channel region and that comprises a second semiconductor having a band gap larger than that of the first semiconductor; and a voltage application means for applying, to the under-channel region, a bias in a direction in which the threshold value voltage becomes higher in the stand-by state than in an operation state.

[0010]

As a result, even when the hetero junction is used to increase the impurity concentration in the lower region of the channel region in the semiconductor layer, an increase in the threshold voltage in the operating state can be suppressed while reducing the substrate bias coefficient. Thus, in the stand-by state, the threshold voltage can be increased to suppress the off leakage current. As a result, an improved driving force by the reduction in the threshold voltage in the operating state as well as suppressed off leakage current by the increase in the threshold voltage by the use of the substrate bias in the stand-by state can be both realized. Thus, the semiconductor device can be operated with a higher speed and lower power consumption.

[0011]

The semiconductor device further comprises a cap layer comprising a third semiconductor that is provided between the channel region and the gate insulator in the semiconductor layer and that has a band gap larger than that of the first semiconductor. As a result, the channel region can be provided with a buried channel structure, thus increasing the variation width of the threshold voltage depending on the change in the substrate bias. Thus, an effect for improving the driving force in the operating state and an effect for suppressing the off leakage current by the increase in the threshold

voltage in the stand-by state can be provided more remarkably.

[0012]

When the first semiconductor is a semiconductor having a composition represented by $Si_{1-x-y}Ge_xC_y$ ($0 \leqq x < 1$, $0 \leqq y < 1$), it is preferable that the second semiconductor is Si. As a result, the manufacture process of Si can be directly used to realize a high-performance hetero junction type MISFET.

[0013]

When the first semiconductor is a semiconductor having a composition represented by $Si_{1-x-y}Ge_xC_y$ ($0 \leqq x < 1$, $0 \leqq y < 1$), it is preferable that the cap layer is made of Si.

[0014]

An insulating layer is provided under the semiconductor layer. This makes it easy to separate and insulate the body region from the exterior on the SOI substrate, thus adjusting the voltage in each body region easily.

[0015]

The source region and the drain region are a p-type source region and a p-type drain region, respectively; and the channel region is a channel region for a p channel. As a result, a semiconductor device functioning as a p channel type MIS transistor is obtained.

[0016]

In this case, the first semiconductor is a semiconductor comprising Si and Ge as components; and the p channel is a buried channel. As a result, the fact that a MIS transistor having a buried channel structure is susceptible to the change in the substrate bias can be used to realize both of a reduced threshold voltage and the suppression of a reduced substrate bias coefficient.

[0017]

The source region and the drain region are an n-type source region and an n-type drain region, respectively; and the channel region is a channel region for an n channel. As a result, a semiconductor device functioning as an n channel type MIS transistor is obtained.

[0018]

In this case, the first semiconductor is a semiconductor comprising Si and C as components; and the n channel is a buried channel. As a result, the fact that a

MIS transistor having a buried channel structure is susceptible to the change in the substrate bias can be used to realize both of a reduced threshold voltage and the suppression of a reduced substrate bias coefficient.

[0019]

When the first semiconductor is a semiconductor having a composition represented by $Si_{1-x-y}Ge_xC_y$ ($0 \leqq x < 1$, $0 \leqq y < 1$) and the under-channel region is doped with boron, the channel region has a composition including Ge or C. Thus, deterioration of the characteristic of the gate insulator due to the diffusion of boron into the channel layer can be suppressed from being caused, for example.

[0020]

The semiconductor device further comprises: another one semiconductor layer provided on the substrate; another one gate insulator provided on the another one semiconductor layer; another one gate electrode provided on the another one gate insulator; an n-type source region and an n-type drain region provided at both sides of the another one gate electrode in the another one semiconductor layer; a channel region for n channel comprising the first semiconductor which is provided in a region in the another one semiconductor layer which is positioned between the n-type source region and the n-type drain region; and another one under-channel region that is provided under the channel region for n channel and that comprises the second semiconductor; and another one voltage application means for applying, to the another one under-channel region, a bias in a direction in which the threshold value voltage becomes higher in the stand-by state than in an operation state. As a result, a semiconductor device functioning as a complementary semiconductor device is obtained.

[0021]

When the first semiconductor is a semiconductor comprising Si and Ge as components, the p channel is a buried channel and the n channel is a surface channel. As a result, the n channel type MIS transistor can maintain the same characteristic as that of the Si-VT type MIS transistor and the p channel type MIS transistor can realize both of high speed operation and low power consumption.

[0022]

The first semiconductor is a semiconductor comprising Si, Ge, and C as components; and the p channel and the n channel are both buried channels. As a

result, both of the n channel type MIS transistor and the p channel type MIS transistor can realize both of high speed operation and low power consumption.

[0023]

[Embodiments of the Invention]

The present invention realizes a lowered threshold voltage Vth and an increased substrate bias coefficient γ at the same time by utilizing a hetero barrier caused by band discontinuity developed at a heterojunction in the channel region, thereby providing VTMIS devices which operate at a higher driving current with a reduced power consumption. Hereinafter, embodiments of the present invention will be described one by one with reference to the accompanying drawings.

[0024]

(First embodiment)

Figs. 1(a) and 1(b) are a sectional view and a plan view, respectively, of a p-channel heterojunction type VTMIS transistor (hereinafter referred to as "pHVTMISFET") having a SiGe layer used as a channel according to a first embodiment of the present invention.

[0025]

As shown in Figs. 1(a) and 1(b), the pHVTMISFET of the subject embodiment includes a p-type Si substrate 10, a Si buffer layer 13 of about 10 nm thickness epitaxially grown on the Si substrate 10 by the UHV-CVD process, a SiGe film 14 (Ge content: 30%) of about 15 nm thickness epitaxially grown on the Si buffer layer 13 by the UHV-CVD process, and a Si cap layer 15 of about 5 nm thickness epitaxially grown on the SiGe film 14 by the UHV-CVD process.

[0026]

The pHVTMISFET further includes a gate insulator 16 of about 6 nm thickness consisting of a silicon oxide film provided on the Si cap layer 15, and a gate electrode 17 provided on the gate insulator 16. A source region 20a and a drain region 20b, which contain a high concentration of a p-type impurity, are provided in regions of the Si buffer layer 13, the SiGe film 14, and the Si cap layer 15 situated on both sides of the gate electrode 17 and are surrounded by a device isolation region 30. A region of the Si substrate 10 defined between the source region 20a and the drain region 20b constitutes a Si body region 22 containing an n-type impurity, while a region of the Si buffer layer 13 located immediately above the Si body region 22

constitutes an n^-Si region 23 containing a low concentration of the n-type impurity. A region of the SiGe film 14 defined between the source region 20a and the drain region 20b constitutes a SiGe channel region 24 containing a relatively low concentration of the n-type impurity, while a region of the Si cap layer 15 located immediately under the gate insulator 16 constitutes a Si cap region 25 containing a low concentration of the n-type impurity. The pHVTMISFET is provided with a gate contact 25 connecting the gate electrode 17 to the wiring located thereabove, a source contact 26a electrically connecting the source region 20a to the wiring located thereabove, a drain contact 26b electrically connecting the drain region 20b to the wiring located thereabove, and a body contact 27 electrically connecting the Si body region 22 to the wiring located thereabove. This body contact 27 is a conductive member for applying an independent bias (voltage) to the Si body region 22. The channel length of the gate electrode 17 is about 0.3 μm.

[0027]

Specifically, the pHVTMISFET of the subject embodiment is structured to be capable of controlling the state of an energy band in a section cutting through the gate electrode 17, gate insulator 16, Si cap layer 25, SiGe channel region 24, n^-Si layer 23, and Si body region 22 by means of a voltage applied to the gate electrode 17 (gate voltage Vg) and a voltage applied to the body region 22 through the body contact 27 (substrate bias Vbs).

[0028]

Here, in p-channel MISFETs in general, a negative voltage applied to the body region serves as a forward substrate bias (bias in such a direction as to lower the threshold voltage) and a positive voltage serves as a reverse substrate bias (bias in such a direction as to raise the threshold voltage). In n-channel MISFETs in general, a positive voltage applied to the body region serves as a forward substrate bias while a negative voltage serves as a reverse substrate bias. Accordingly, in a p-channel MISFET, when a positive voltage is applied to the body region, the reverse substrate bias increases as the value of the positive voltage increases, while when a negative voltage is applied to the body region, the forward substrate bias increases as the absolute value of the negative voltage increases. In an n-channel MISFET, on the other hand, when a negative voltage is applied to the body region, the reverse substrate bias increases as the absolute value of the negative voltage increases, while when a

positive voltage applied to the body region, the forward substrate bias increases as the value of the positive voltage increases.

[0029]

In the subject embodiment, a substrate bias control circuit as shown in Fig. 15 applies a substrate bias Vbs to the p-well (p-body region) of nHVTMISFET so that the threshold voltage is lowered in the operating state or raised in the stand-by state. The region to be applied with the substrate bias is sufficient to be located below the channel region and is a region called "well" or "body region". This region is a p-type region in an n-channel transistor, or an n-type region in a p-type region.

[0030]

Figs. 2(a), 2(b) and 2(c) are each a diagram showing an energy band obtained in a section cutting through the gate electrode 17, gate insulator 16, Si cap layer 25, SiGe channel region 24, n^-Si layer 23, and Si body region 22 in the built-in state, in the gate bias-applied state (operating state), and in the gate bias-free state (stand-by state), respectively.

[0031]

As shown in Fig. 2(a), when the transistor is in the built-in state, the band gap in the SiGe channel region 24 having a Ge content of 30% is about 220 meV less than that in the Si cap layer 25 and n^-Si layer 23, so that a hetero barrier at a valence band edge, which is capable of confining holes, is developed between the SiGe channel region 24 and the Si cap layer 25 and between the SiGe channel region 24 and the n^-Si layer 23. With the gate electrode 17 doped with a p-type impurity, the energy at a valence band edge in the portion of the SiGe channel region 24 contacting the Si cap layer 25 becomes particularly high in a bias-free state (in the built-in state), so that the valence band is formed with a dent portion, which is suitable for confinement of holes, in the portion of the SiGe channel region 24 adjoining the hetero barrier.

[0032]

Thus, merely with application of a faint gate bias Vg, the band can be bent to form a p-channel in the portion of the SiGe channel region 24 adjoining the Si cap layer 25, thereby making it easy to lower the threshold voltage Vth. In the subject embodiment, the substrate bias Vbs is 0 V in the operating state. The SiGe channel region 24 is formed at a location spaced from the gate insulator 16 by the thickness of the Si cap layer 25 and, hence, the SiGe-pHVTMISFET according to the present

invention has a so-called "buried channel structure".

[0033]

With a design to lower the threshold voltage Vth, the negative voltage to be applied to the gate electrode 17 for on-operation needs to be small enough to allow a design to be made such that an inversion layer can hardly be developed in the portion of the Si cap layer 25 adjoining the gate insulator 16. As a result, the so-called parasitic channel, which would otherwise be formed in other portion than the SiGe channel region 24, can be effectively prevented from being developed. Thus, the MISFET can be made operable at a lower voltage as well as at a higher speed by utilizing the fast mobility of holes, which is characteristic of the SiGe channel region 24.

[0034]

As shown in Fig. 2(c), when the pHVTMISFET is in the stand-by state, the transistor is applied with a large positive substrate bias Vbs (reverse bias), so that the valence band edge is largely bent downwardly. This means that the potential at the valence band edge in the channel region is increased relative to the potential at the valence band edge in the source·drain region (that is, the barrier is heightened). Accordingly, the threshold voltage, which is a voltage to be applied to the gate electrode 17 to turn the pHVTMISFET on, is increased, resulting in reduced leakage current (off-leakage current) when the gate bias is 0 V.

[0035]

It should be noted that the pHVTMISFET may be used in such manner that the threshold voltage is lowered in the operating state by application of a forward (negative) substrate bias Vbs and raised in the stand-by state by application of a substrate bias Vbs of 0 V.

[0036]

- Substrate bias coefficient -

Moreover, in the subject embodiment, the substrate bias coefficient γ, which is the ratio of a change in threshold voltage Vth to a change in substrate bias Vbs, can be increased even if the threshold voltage Vth is lowered. Therefore, the threshold voltage of the MIS transistor can be shifted largely in response to the change in the substrate bias. This has been proved from the following data.

[0037]

Figs. 3(a) and 3(b) are each a diagram showing the result of simulation of the potential at a valence band edge in a conventional Si-pVTMISFET and in the SiGe-pHVTMISFET of the present invention, respectively. Each of Figs. 3(a) and 3(b) plots the depthwise level from the top surface of the substrate as the abscissa and the potential as the ordinate. Note that in a p-channel MISFET the potential (potential relative to the transit of holes) increases as it grows toward the negative side since the holes work as carriers. In both of the conventional Si-pVTMISFET and the SiGe-pHVTMISFET of the present invention, the impurity concentration in the body region is 1×10^{18} cm^{-3}, the substrate bias Vbs varies from 0.6 V (reverse bias) to –0.6 V (forward bias), and the gate bias Vg is 0 V. In Figs. 3(a) and 3(b), the dotted lines plot the potential at the Si channel and the potential at the SiGe channel, respectively.

[0038]

As can be seen from the comparison between Figs. 3(a) and 3(b), the potential at the SiGe channel of the pHVTMISFET according to the present invention is lower than the potential at the Si channel formed in a region adjacent the interface with the gate insulator of the conventional Si-pVTMISFET. This is attributed to the band gap of SiGe smaller than that of Si.

[0039]

Further, the potential gradient Δ of the SiGe channel shown in Fig. 3(b) is larger than the potential gradient of the Si channel shown in Fig. 3(a). That is, the dependency of a change in the potential at the valence band edge in the SiGe channel on the substrate bias Vbs is higher than that in the Si one. This means that the SiGe-pHVTMISFET has a greater substrate bias coefficient γ than the Si-pVTMISFET. This can be reasoned as follows. That is, the conventional Si-pVTMISFET has the Si channel formed in a portion adjoining the gate insulator, stated otherwise, in a portion proximate to the top surface of the semiconductor substrate, while the pHVTMISFET according to the present invention has a so-called buried channel structure in which the SiGe channel is formed at a location spaced from the gate insulator by the thickness of the Si cap layer and, hence, a greater influence is exerted on the SiGe channel by the substrate bias Vbs.

[0040]

Fig. 4 is a diagram showing the result of simulation of dependency of the channel potential on the substrate bias in each of the conventional Si-pVTMISFET and

the SiGe-pHVTMISFET according to the present invention. This figure plots the substrate bias Vbs as the abscissa and the channel potential as the ordinate. Note that since holes work as carriers in a p-channel MISFET, the potential (potential relative to the transit of holes) increases as it grows toward the negative side. In both of the conventional Si-pVTMISFET and the SiGe-pHVTMISFET according to the present invention, the impurity concentration in the body region is varied to have values of 1×10^{18} cm^{-3}, 2×10^{18} cm^{-3}, and 5×10^{18} cm^{-3}, and the gate bias Vg is 0 V.

[0041]

As more clearly shown in this figure, a change in channel potential (the gradient of each line) relative to a change in substrate bias Vbs in the SiGe channel of the present invention is larger than that in the conventional channel. That is, both the lowering of threshold voltage Vth and the increasing of substrate bias coefficient γ can be realized. By constituting the VTMISFET by the SiGe heterojunction type MISFET having the SiGe channel, a synergistic and remarkable effect can be obtained,

[0042]

Also, as can be understood from the fact that the potential of the SiGe channel except a reversely biased region that is strongly biased with the substrate biasVth (Vbs is 0.3 V or more) is lower than that of the Si channel, the threshold voltage Vth of the SiGe-pHVTMISFET is lower than that of the Si-pVTMISFET and, hence, the threshold voltage Vth can be kept low even when the impurity concentration of the body region is rendered high. It can also be understood from these facts that the SiGe-pHVTMISFET according to the present invention can realize a still larger substrate bias coefficient γ and is less affected by the short channel effect.

[0043]

While the Si cap layer 25 has a thickness of 5 nm in the subject embodiment, the thickness of the Si cap layer 25 is preferably within the range of not less than 1 nm and not more than 10 nm. Reasons therefor include: the Si cap layer 25 needs to have a thickness of about 1 nm for the gate insulator to be formed stably by thermal oxidation of the Si cap layer 25; if the Si cap layer is too thick, the SiGe channel region 24 becomes remoter from the gate insulator 16, so that the degree of lowering of the threshold voltage Vth is decreased, though the substrate bias coefficient γ is increased; and the short channel effect might become conspicuous.

[0044]

Although the SiGe channel region 24 preferably has a higher Ge content in lowering the threshold voltage Vth to a greater degree, too high a Ge content makes a critical film thickness impractically thin, the critical thickness being a thickness critical to allowing strain caused by Si-SiGe lattice mismatch to be relaxed. Thus, the Ge content in the SiGe channel region is preferably within the range of not less than 15% and not more than 40%. The thickness of the SiGe channel region 24 is preferably within the range of not less than 3 nm and not more than 20 nm. As the thickness of the Si buffer layer 13 increases, the substrate bias coefficient γ decreases and the threshold voltage Vth lowers. Since too thick Si buffer layer 13 causes the threshold voltage Vth to lower too much, the thickness of the Si buffer layer 13 is preferably not less than 0 nm and not more than 20 nm.

[0045]

The following description will compare the basic characteristics, namely characteristics under the condition where the substrate bias Vbs is not applied, of the SiGe-HVTMISFET of the subject embodiment to those of the conventional Si-VTMISFET.

[0046]

Fig. 5 is a diagram showing the Vg-Id characteristic of the conventional Si-pVTMISFET and that of the SiGe-pHVTMISFET of the present invention for comparison. In this figure, in each of the transistors the impurity concentration in the substrate is 1×10^{18} cm^{-3} and the substrate bias Vbs is 0 V. As has already been described, the SiGe-pHVTMISFET is found to exhibit a lowered threshold voltage Vth. Also, as shown in the lower-left section of this figure, the SiGe-pHVTMISFET exhibits an increased mutual conductance (gm). This reflects the hole mobility in the SiGe channel higher than that in the Si channel.

[0047]

Figs. 6(a) and 6(b) are diagrams showing changes in the Vg-Id characteristic of the conventional Si-pVTMISFET and those in the Vg-Id characteristic of the SiGe-pHVTMISFET of the present invention, respectively, for comparison. In each of Figs. 6(a) and 6(b), the gate overdrive voltage (Vg - Vth) is varied as a parameter. As can be seen from these figures, a saturation drain current obtained by the SiGe-pHVTMISFET of the present invention with the gate overdrive voltage exceeding the threshold voltage Vth is about 1.2 times as large as that obtained by the

conventional Si-pVTMISFET.

[0048]

Fig. 7 is a diagram showing the effective hole mobility under application of a low electric field in the conventional Si-pVTMISFET and that in the SiGe-pHVTMISFET of the present invention for comparison. The SiGe-pHVTMISFET of the present invention exhibits hole mobility about twice as high as that of the conventional Si-pVTMISFET. Thus, the use of SiGe as a channel in a VTMISFET makes it possible not only to lower the threshold voltage Vth and increase the substrate bias coefficient γ but also to obtain a high hole mobility, thereby exhibiting the effect of improving the mutual conductance (gm) and increasing the saturation drain current as already described. Hence, the use of SiGe as a channel is very effective in making the transistor operable at a higher speed.

[0049]

Figs. 8(a) and 8(b) are diagrams showing Vg-Id characteristics of the conventional Si-pVTMISFET in the case where the impurity concentration in the body region is 2×10^{17} cm^{-3} and 5×10^{17} cm^{-3}, respectively. Figs. 9(a) to 9(c) are diagrams showing Vg-Id characteristics of the SiGe-pHVTMISFET of the present invention in the case where the impurity concentration in the body region is 2×10^{17} cm^{-3}, 5×10^{17} cm^{-3}, and 1×10^{18} cm^{-3}, respectively. Figs. 8(a) and 8(b) and Figs. 9(a) to 9(c) plot the respective Vg-Id characteristic curves in the case where the substrate bias Vbs varies stepwise by 0.2 V from –0.6 V to 1 V. As can be seen from Fig. 9(b) for example, by controlling the substrate bias Vbs so that it assumes –0.6 V in the operating state of the MISFET and 0 V in the stand-by state, there can be obtained a high drive current in the operating state and a high threshold voltage Vth in the stand-by state. As well, by controlling the substrate bias Vbs so that it assumes 0 V in the operating state of the MISFET and 1 V in the stand-by state, there can also be obtained a high drive current in the operating state and a high threshold voltage Vth in the stand-by state.

[0050]

It can be understood from comparisons among Figs. 8(a) and 8(b) and Figs. 9(a) to 9(c) that when the SiGe-pHVTMISFET of the present invention and the conventional Si-pVTMISFET have equal impurity concentration in their respective body regions and are applied with equal substrate bias Vbs, the SiGe-pHVTMISFET of the present invention has a threshold voltage lower than that of the conventional

Si-pVTMISFET and exhibits a change in Vg-Id characteristic relative to a change in substrate bias Vbs within a range larger than that in the conventional Si-pVTMISFET. Specifically, the provision of a SiGe channel in a VTMISFET was proved to enable the threshold voltage Vth to lower and allow an increased threshold voltage shift (substrate bias coefficient γ) relative to substrate bias Vbs to occur.

[0051]

The threshold voltage Vth of the SiGe-pHVTMISFET of the present invention lowers markedly when a forward substrate bias Vbs is applied. This means that application of a forward substrate bias Vbs brings about an increased drain current Id. Such a large reduction in threshold voltage Vth caused by application of a forward substrate bias is attributed to a low potential relative to transit of holes in the SiGe channel region as viewed from the source side due to SiGe having a band gap smaller than that of Si.

[0052]

On the other hand, the SiGe-pHVTMISFET of the present invention as well as the conventional Si-pVTMISFET exhibit an increase in substrate bias coefficient γ as the impurity concentration in the body region is raised. Further, the difference in substrate bias coefficient γ between the SiGe-pHVTMISFET of the present invention and the conventional Si-pVTMISFET becomes more significant as the impurity concentration in the body region is raised.

[0053]

Fig. 10 is a diagram showing dependency of the threshold voltage on the substrate bias in each of the conventional Si-pVTMISFET and the SiGe-pHVTMISFET of the present invention with the impurity concentration in the body region used as a parameter. With rising impurity concentration in the body region, the threshold voltage Vth rises and the substrate bias coefficient γ increases. Also, it can be well understood that the provision of the SiGe channel makes it possible to lower the threshold voltage and increase the substrate bias coefficient γ. Further, the threshold voltage Vth of the SiGe-pHVTMISFET lowers (varies toward the positive side) markedly particularly when a forward substrate bias (negative voltage) is applied. This is attributed to the potential of the SiGe channel lower than that of the Si channel as described earlier and hence indicates that the SiGe-pHVTMISFET has a higher drive current.

[0054]

Figs. 11(a) and 11(b) are diagrams showing the Vg-Id characteristic of the conventional Si-pVTMISFET and that of the SiGe-pHVTMISFET of the present invention under the condition where their threshold voltages are equalized to each other, with the substrate bias being used as a parameter, respectively. In Figs. 11(a) and 11(b), the impurity concentration in the body region of each of the VTMISFETs is adjusted so that the threshold voltages Vth of two VTMISFETs are equal to each other when the substrate bias Vbs is 0 V. In this case, the impurity concentration in the body region of the Si-pVTMISFET is 5×10^{17} cm^{-3}, while that in the body region of the SiGe-HVTMISFET is 1×10^{18} cm^{-3}, which is twice as high as 5×10^{17} cm^{-3}.

[0055]

Thus, since the channel region of the SiGe-pHVTMISFET of the present invention is formed of SiGe, the threshold voltage of the SiGe-pHVTMISFET can be adjusted to a value substantially equal to the threshold voltage of the Si-pVTMISFET, with the impurity concentration in the body region of the SiGe-pHVTMISFET being kept high. As a result, the SiGe-pHVTMISFET realizes a very large substrate bias coefficient γ as compared to the Si-pVTMISFET. This is attributed to the features that: the impurity concentration in SiGe body region 23 can be kept high; and the SiGe-pHVTMISFET can employ the buried channel structure. Thus, the SiGe-pHVTMISFET realized by the present invention is a high-performance transistor capable of generating a high driving current by decreasing the substrate bias Vbs in the operating state and of reducing the off-leakage current by increasing the substrate bias Vbs in the stand-by state.

[0056]

Fig. 12 is a diagram expressing the Vg-Id characteristics of the conventional Si-pVTMISFET and SiGe-pHVTMISFET of the present invention shown in Fig. 11 as respective on-current Ion vs. off-leakage current Ioff characteristics. The drain voltage of each VTMISFET is fixed to –1 V. This figure plots on-current Ion (drain current) as the abscissa and off-current Ioff as the ordinate. In this figure, ○ and □ represent on-current Ion data and off-leakage current Ioff data, respectively, of the conventional Si-pVTMISFET, while ● and ■ represent on-current Ion (drain current) data and off-leakage current Ioff data, respectively, of the SiGe-pHVTMISFET of the present invention. Here, ○ and ● are obtained

from respective Vg-Id characteristic curves in the case where the substrate bias Vbs is –0.4 V in the operating state and 0.8 V in the stand-by state, respectively, while □ and ■are obtained from respective Vg-Id characteristic curves in the case where the substrate bias Vbs is 0 V in the operating state and 0.8 V in the stand-by state, respectively.

[0057]

As seen from Fig. 12, when the conventional Si-pVTMISFET and the SiGe-pHVTMISFET of the present invention exhibit off-leakage currents of equal value, an on-current Ion obtained in the SiGe-pHVTMISFET of the present invention (○ and □) is higher than that obtained in the conventional Si-pVTMISFET (● and ■). This is attributed to a large shift in threshold voltage caused by an increased substrate bias coefficient γ possessed by the SiGe-pHVTMISFET having the buried channel structure with a high impurity concentration in the body region and to the hole mobility in the SiGe channel region 24 higher than that in the Si channel region. When the substrate bias Vbs is applied forwardly (Vbs = -0.4 V) in the operating state, the difference in on-current Ion between the conventional Si-pVTMISFET and the SiGe-pHVTMISFET of the present invention becomes conspicuous. Stated otherwise, a higher Ion/Ioff ratio can be obtained in the SiGe-pHVTMISFET of the present invention.

[0058]

That is, application of a forward substrate bias Vbs in the operating state is effective in obtaining a higher on-current Ion (drain current Id) in the SiGe-pHVTMISFET of the present invention. This is because the difference in threshold voltage Vth between the operating state and the stand-by state is conspicuously large due to a low potential relative to transit of carriers in the SiGe channel region 24. Conversely, this means that in a MIS transistor adapted to be driven under application of a forward substrate bias Vbs in the operating state, it is effective that the channel region thereof is formed of a material having a band gap smaller than that of the cap layer thereof and, at the same time, has the buried channel structure.

[0059]

As described above, the subject embodiment is capable of increasing the substrate bias coefficient γ, which is the ratio of a change in the threshold voltage Vth

to a change in the substrate bias Vbs, even when the threshold voltage Vth is lowered and, therefore, the subject embodiment is capable of largely shifting the threshold voltage of the VTMIS transistor in response to the change in substrate bias. For this reason, the subject embodiment is capable of enhancing the drive current in the operating state while reducing the off-leakage current in the stand-by state. That is, the subject embodiment is effective as a transistor that operates at a high speed with low power consumption.

[0060]

Further, since the subject embodiment is capable of keeping the threshold voltage Vth low even when the impurity concentration in the body region is raised, the subject embodiment has an improved resistance to the short channel effect thereby making it possible to keep the operation of even a short gate-length transistor normal. For this reason, the subject embodiment provides for higher integration and higher performance.

[0061]

While the subject embodiment is an embodiment wherein the present invention is applied to a pHVTMISFET having a SiGe channel region, it is needless to say that the present invention is also applicable to a HVTMISFET having a SiC channel region (particularly of the n-channel type) containing a trace amount of C or a SiGeC channel region (of any one of the p-channel type and the n-channel type) containing a trace amount of C on a Si substrate. Where the present invention is applied to such a HVTMISFET having a SiC channel region containing a trace amount of C on a Si substrate, it is possible to realize an n-channel type MISFET (nHVTMISFET) functioning as a transistor that operates at a high speed with low power consumption by utilizing large band discontinuity (hetero barrier) developed at a conduction band edge.

[0062]

While the subject embodiment uses the bulk Si substrate, it is possible to use a SOI substrate. Use of such a SOI substrate makes it easy to isolate the body regions of respective HVTMISFETs to inhibit electrical connection therebetween and, hence, substrate bias Vth control on a HVTMISFET-by-HVTMISFET basis becomes easy.

[0063]

(Second embodiment)

This embodiment is an embodiment wherein the present invention is applied to a complementary HVTMIS device having SiGe channels.

[0064]

Figs. 13(a), 13(b) and 13(c) are views showing the structure of the cHVTMIS device according to this embodiment, an energy band diagram showing a band state of a pHVTMISFET under application of a gate bias (in the operating state), and an energy band diagram showing a band state of an nHVTMISFET under application of a gate bias (in the stand-by state), respectively.

[0065]

As shown in Fig. 13(a), the cHVTMIS device according to the subject embodiment includes a p-type Si substrate 10, a buried oxide film 11 formed by implanting oxygen ions into the Si substrate or by a like process, a semiconductor layer 30 formed on the buried oxide film 11 for a p-channel HVTMISFET (pHVTMISFET), and a semiconductor layer 80 formed on the buried oxide film 11 for an n-channel HVTMISFET (nHVTMISFET). The semiconductor layer 30 comprises an upper Si film 12, a Si buffer layer 13 of about 10 nm thickness epitaxially grown on the upper Si film 12 by the UHV-CVD process, a SiGe film 14 (Ge content: 30%) of about 15 nm thickness epitaxially grown on the Si buffer layer 13 by the UHV-CVD process, and a Si cap layer 15 of about 5 nm thickness epitaxially grown on the SiGe film 14 by the UHV-CVD process, these films and layers forming an upper part of a SOI substrate. On the other hand, the semiconductor layer 80 comprises an upper Si film 52 formed on the buried oxide film 11, a Si buffer layer 53 epitaxially grown on the upper Si film 52 by the UHV-CVD process, a SiGe film 54 epitaxially grown on the Si buffer layer 53 by the UHV-CVD process, and a Si film 55 epitaxially grown on the SiGe film 54 by the UHV-CVD process. The thicknesses of Si buffer layer 53, SiGe film 54 and Si film 55 of the semiconductor layer 80 are equal to the thicknesses of Si buffer layer 13, SiGe film 14 and Si cap layer 15 of the semiconductor layer 30, respectively.

[0066]

The cHVTMIS device further includes gate insulators 16 and 56 formed of respective silicon oxide films on the semiconductor layers 30 and 80, respectively, gate electrodes 17 and 57 provided on the gate insulators 16 and 56, respectively, and

sidewalls 18 and 58 each formed on both sides of a respective one of the gate electrodes 17 and 57. A source region 20a and a drain region 20b, which contain a high concentration of a p-type impurity, are provided in regions of the semiconductor layer 30 situated on the both sides of the gate electrode 17 in plan view. A source region 60a and a drain region 60b, which contain a high concentration of an n-type impurity, are provided in regions of the semiconductor layer 80 situated on the both sides of the gate electrode 57 in plan view. A region of the upper Si film 12 located between the source region 20a and the drain region 20b defines therein a Si body region 22 containing a high concentration of the n-type impurity, while a region of the Si buffer layer 13 located between the source region 20a and the drain region 20b defines therein an n^-Si region 23 containing a low concentration of the n-type impurity. A region of the SiGe film 14 located between the source region 20a and the drain region 20b defines therein a SiGe channel region 24 containing a low concentration of the n-type impurity, while a region of the Si film 15 located between the source region 20a and the drain region 20b defines therein a Si cap layer 25 containing a low concentration of the n-type impurity. On the other hand, a region of the upper Si film 52 located between the source region 60a and the drain region 60b defines therein a Si body region 62 containing a high concentration of the p-type impurity, while a region of the Si buffer layer 53 located between the source region 60a and the drain region 60b defines therein a p^-Si region 63 containing a low concentration of the p-type impurity. A region of the SiGe film 54 located between the source region 60a and the drain region 60b defines therein a SiGe channel region 64 containing a low concentration of the p-type impurity, while a region of the Si film 55 located between the source region 60a and the drain region 60b defines therein a Si cap layer 65 containing a low concentration of the p-type impurity.

[0067]

Though not shown, the substrate is provided thereon with an interlayer dielectric, contacts extending through the interlayer dielectric to contact the source·drain regions 20a, 20b, 60a and 60b, and source·drain electrodes connected to the respective contacts and extending on the interlayer dielectric, for example.

[0068]

In the fabrication process for the cHVTMIS device according to the subject embodiment, the upper Si films (body regions) forming part of respective SOI

substrates are an n^+Si layer (in the pHVTMISFET region) and p^+Si layer (in the nHVTMISFET region), respectively, the n^+Si layer and p^+Si layer being doped with respective impurities to a concentration of about 1×10^{18} atoms·cm^{-3} by ion implantation prior to crystal growth, while any one of the Si buffer layers, SiGe channel regions and Si cap layers in an as-grown state is an undoped layer not doped with an impurity. At that time, the thicknesses of each Si buffer layer, each SiGe channel layer and each Si cap layer are 10 nm, 15 nm and 5 nm, respectively. The Ge content in the SiGe channel regions is 30%. After the completion of crystal growth of the SiGe films and Si cap layers, a portion around the SiGe channel region in the nHVTMISFET is doped with the p-type impurity to a concentration of about 1×10^{17} atoms·cm^{-3} by ion implantation. As well, a portion around the SiGe channel region in the pHVTMISFET is doped with the n-type impurity to a concentration of about 1×10^{17} atoms·cm^{-3} by ion implantation. Note that the SiGe films and the Si cap layers may be left undoped. Subsequently, the Si cap layers as the topmost layers are thermally oxidized to form silicon oxide films for use as the gate insulators, and then the n-type gate electrode formed of polysilicon heavily doped with the n-type impurity and the p-type gate electrode formed of polysilicon heavily doped with the p-type impurity are formed on the respective gate insulators. Thereafter, the n^+-type source·drain regions heavily doped with the n-type impurity by ion implantation and the p^+-type source·drain regions heavily doped with the p-type impurity by ion implantation are formed on both sides of respective gate electrode, followed by formation of source electrode and drain electrode above respective one of the n^+-type source·drain regions and the p^+-type source·drain regions, respectively. Though not shown, the upper Si films (Si body regions 22 and 62) are connected to respective overlying wiring via respective contacts.

[0069]

As shown in Fig. 13(b), in the pHVTMISFET the substrate bias Vbs is 0 bias or a forward bias in the operating state and application of a gate bias causes a p-channel having a low potential relative to transit of holes to be formed in the SiGe channel region 24, as has been described in the first embodiment.

[0070]

As shown in Fig. 13(c), in the nHVTMISFET the substrate bias Vbs is 0 bias or a forward bias in the operating state and application of a gate bias causes an

n-channel to be formed in the Si cap layer 65. Since conduction band discontinuity can hardly be developed at the heterojunction between Si and SiGe, the nHVTMISFET of the cHVTMIS device according to the subject embodiment has an operating function equivalent to that of the conventional n-channel Si-VTMISFET.

[0071]

The construction of the cHVTMIS device according to the subject embodiment has an advantage of enabling a complementary HVTMIS device to be fabricated by a simplified process.

[0072]

Particularly where boron is used as the impurity with which the Si body region 62 of the nHVTMISFET is doped, the presence of the SiGe channel region 64 between the Si buffer region 63 and the Si cap layer 65 inhibits the diffusion of boron from the Si body region 62 into the Si cap layer 65. Accordingly, the impurity concentration in the channel region formed in a region of the Si cap layer 65 situated adjacent the interface with the gate insulator 56 can be reduced. This is attributed to a lower diffusion coefficient of boron in a SiGe region than in a Si region. As a result, it is possible to lower the threshold voltage Vth of the nHVTMISFET as well as to reduce the deterioration of electron mobility due to scattering by the impurity. Thus, a high drive current can be realized. Further, since the threshold voltage of the nHVTMISFET can be lowered, it is also possible to increase the substrate bias coefficient γ by raising the impurity concentration in the Si body region 62.

[0073]

(Third embodiment)

While the channel regions in the first and second embodiments are formed of SiGe, these channel regions may be formed of $Si_{1-x-y}Ge_xC_y$ having a C (carbon) content of 0.01% to 2% (for example, about 1%). The addition of a trace amount of C in each SiGe channel region further enhances the effect of the SiGe channel region. Though ion implantation into a SiGe crystal has a strong tendency to cause the crystal structure thereof to change undesirably, it is possible to inhibit such an undesirable change of crystal structure caused by ion implantation by forming a channel region of $Si_{1-x-y}Ge_xC_y$.

[0074]

Figs. 14(a), 14(b) and 14(c) are views showing the construction of a

cHVTMIS device according to this embodiment, an energy band diagram showing a band state of a pHVTMISFET under application of a gate bias (in the operating state), and an energy band diagram showing a band state of an nHVTMISFET under application of a gate bias (in the stand-by state). In the subject embodiment the channel regions are formed of $Si_{1-x-y}Ge_xC_y$.

[0075]

The cHVTMIS device shown in Fig. 14(a) can be obtained by substitution of SiGeC films 19 and 59 for the SiGe films 14 and 54, respectively, of the pHVTMISFET and nHVTMISFET shown in Fig. 13 and substitution of SiGeC channel regions 29 and 69 for the SiGe channel regions 24 and 64, respectively, of the pHVTMISFET and nHVTMISFET shown in Fig. 13. The structures of other parts are the same as those of corresponding parts of the cHVTMIS device shown in Fig. 13.

[0076]

As shown in Fig. 14(b) and 14(c), the subject embodiment has buried channels (SiGeC buried p-channel and SiGeC buried n-channel) formed in the pHVTMISFET and the nHVTMISFET, respectively.

[0077]

Fig. 15 is a block circuit diagram showing a circuit configuration for applying a substrate bias Vbs to each of the nHVTMISFET and pHVTMISFET according to the subject embodiment. As shown in this figure, the p-well (p-body region) of the nHVTMISFET and the n-well (n-body region) of the pHVTMISFET are each applied with a substrate bias Vbs by a substrate bias control circuit 50 so that the threshold voltage is lowered in the operating state and raised in the stand-by state. The region to be applied with the substrate bias, which is sufficient to be located below the associated channel region, is called a well or a body region. Such a region is a p-type region in an n-type transistor or an n-type region in a p-type transistor.

[0078]

According to the subject embodiment having the channel regions formed of SiGeC, both valence band discontinuity and conduction band discontinuity (hetero barrier) are allowed to develop at a Si/SiGeC heterojunction thereby forming n-channel and p-channel both of which are of the buried channel structure. That is, since the nHVTMISFET also has a buried channel, this transistor is capable of lowering its threshold voltage Vth as well as of increasing its substrate bias coefficient γ like the

pHVTMISFET according to the first embodiment. Therefore, both the pHVTMISFET and nHVTMISFET can realize a high Ion/Ioff ratio. Moreover, the SiGeC films 19 and 59 for defining the p-channel region (SiGeC channel region 29) and the n-channel region (SiGeC channel region 69), respectively, can be formed by a single epitaxial growth step. This results in reduced fabrication cost.

[0079]

As has been described in the second embodiment, also in the cHVTMIS device of the subject embodiment, the effect of inhibiting the diffusion of boron from the Si body region 62 into the Si cap layer 65 can be exhibited more remarkably by the presence of the SiGeC channel region 69. Conceivably, this is because C atoms fill vacancy causing transient enhanced diffusion of the impurity.

[0080]

[Effect of the Invention]

The present invention allows material having a band gap smaller than that of Si to be introduced in the channel region of the semiconductor device functioning as VTMISFET, thus realizing the lowering of threshold voltage and the increasing of the substrate bias coefficient γ. Thus, both of the high speed operation and low power consumption can be realized.

[Brief Description of the Drawings]

[Figure 1]

Figs. 1(a) and 1(b) are a sectional view and a plan view, respectively, of a heterojunction type pHVTMISFET having a SiGe layer used as a channel according to a first embodiment of the present invention.

[Figure 2]

Figs. 2(a), 2(b) and 2(c) are each a diagram showing an energy band in the case where the transistor is in its built-in state, an energy band in the case where the transistor is applied with a gate bias (in its operating state), and an energy band in the case where the transistor is not applied with the gate bias (in its stand-by state).

[Figure 3]

Figs. 3(a) and 3(b) are each a diagram showing the result of simulation of the potential at a valence band edge in a Si-pVTMISFET and the SiGe-pHVTMISFET.

[Figure 4]

Fig. 4 is a diagram showing the result of simulation of dependency of the

channel potential on the substrate bias in each of the Si-pVTMISFET and the SiGe-pHVTMISFET.

[Figure 5]

Fig. 5 is a diagram showing the Vg-Id characteristic of the Si-pVTMISFET and that of the SiGe-pHVTMISFET for comparison.

[Figure 6]

Figs. 6(a) and 6(b) are diagrams showing changes in the Vg-Id characteristic of the Si-pVTMISFET and those in the Vg-Id characteristic of the SiGe-pHVTMISFET, respectively, for comparison.

[Figure 7]

Fig. 7 is a diagram showing the effective hole mobility under application of a low electric field in the Si-pVTMISFET and that in the SiGe-pHVTMISFET for comparison.

[Figure 8]

Figs. 8(a) and 8(b) are diagrams showing the Vg-Id characteristics of the Si-pVTMISFET in the case where two types of impurity concentrations are used.

[Figure 9]

Figs. 9(a) to 9(c) are diagrams showing the Vg-Id characteristics of the SiGe-pHVTMISFET in the case where two types of impurity concentrations are used.

[Figure 10]

Fig. 10 is a diagram showing dependency of the threshold voltage on the substrate bias in each of the Si-pVTMISFET and the SiGe-pHVTMISFET.

[Figure 11]

Figs. 11(a) and 11(b) are diagrams showing the Vg-Id characteristic of the Si-pVTMISFET and the SiGe-pHVTMISFET under the condition where their threshold voltages are equalized to each other.

[Figure 12]

Fig. 12 is a diagram expressing the Vg-Id characteristics of the Si-pVTMISFET and SiGe-pHVTMISFET shown in Fig. 11 as respective Ion-Ioff characteristics.

[Figure 13]

Figs. 13(a), 13(b) and 13(c) are a sectional view showing the structure of the cHVTMIS device according to the second embodiment, an energy band diagram

showing a band state of a pHVTMISFET in the operating state, and an energy band diagram showing a band state of an nHVTMISFET in the operating state, respectively.

[Figure 14]

Figs. 14(a), 14(b) and 14(c) are a sectional view showing the structure of the cHVTMIS device according to the third embodiment, an energy band diagram showing a band state of a pHVTMISFET in the operating state, and an energy band diagram showing a band state of an nHVTMISFET in the operating state.

[Figure 15]

Fig. 15 is a block circuit diagram showing a circuit configuration for applying a substrate bias Vbs to each of the nHVTMISFET and pHVTMISFET according to the third embodiment.

[Description of the Reference Numerals]

10 Si substrate
11 Buried oxide film
12 Upper Si film
13 Si buffer layer
14 SiGe film
15 Si cap layer
16 Gate insulator
17 Gate electrode
20a Source region
20b Drain region
22 Si body region
23 n^-Si region

【Name of the Document】 DRAWINGS

Fig. 1(a)

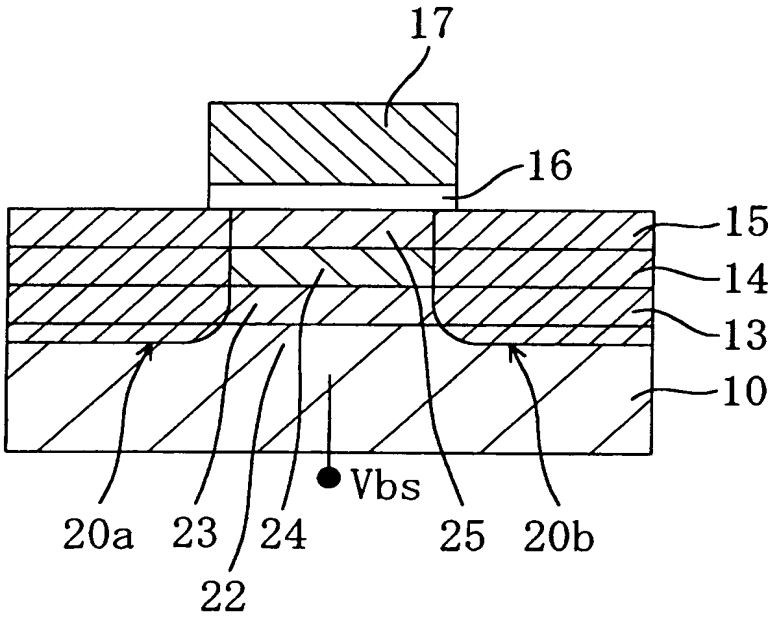


Fig. 1(b)

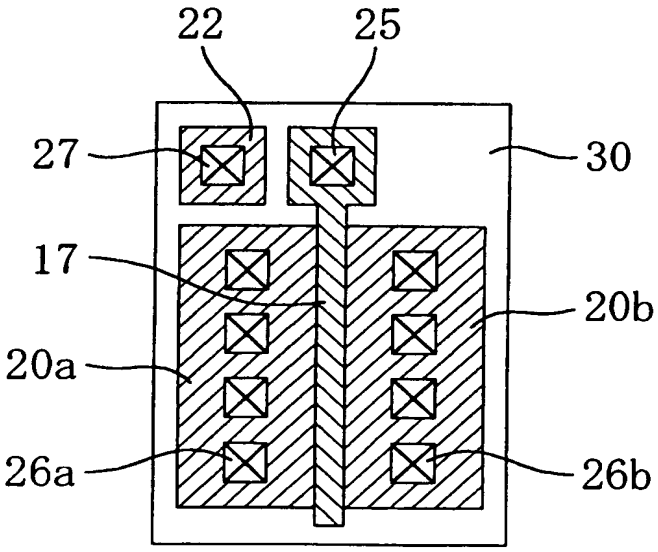


Fig. 2(a)

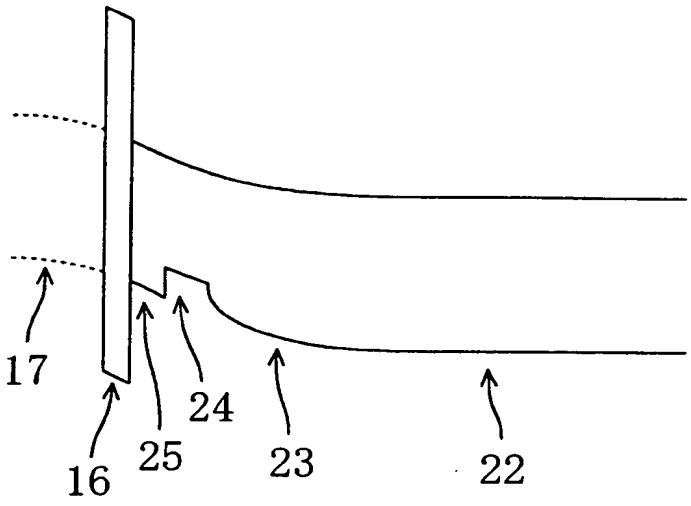


Fig. 2(b)

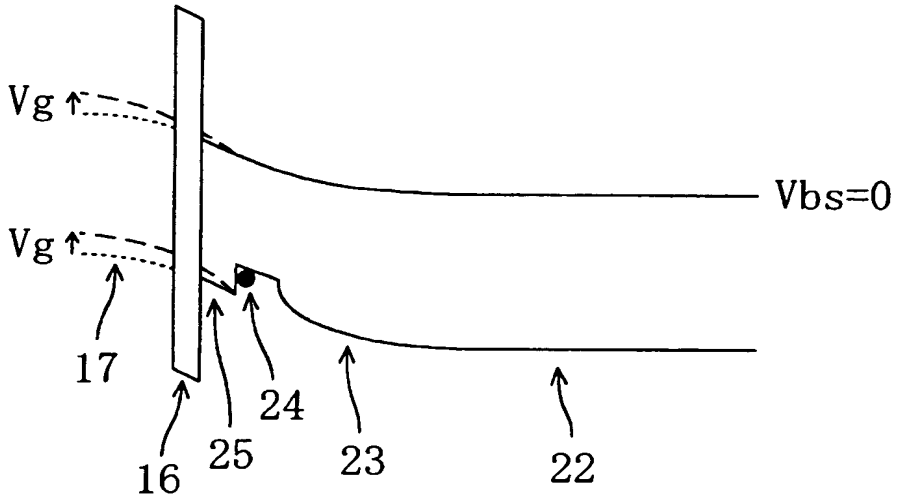


Fig. 2(c)

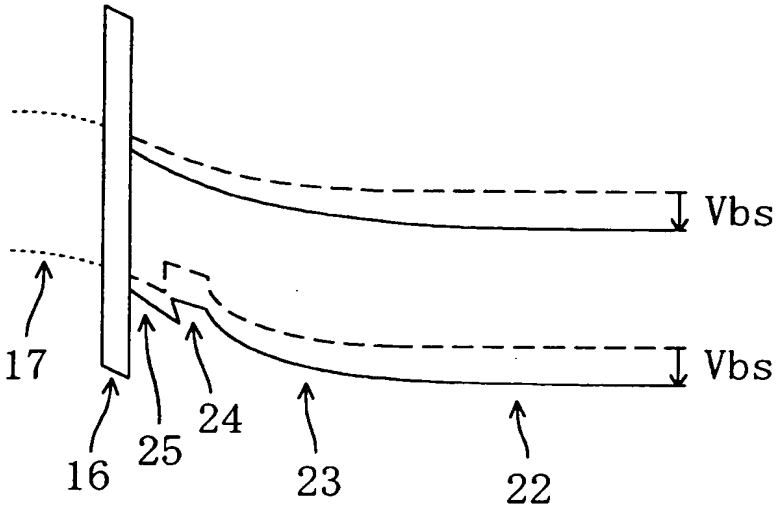


Fig. 3(a)

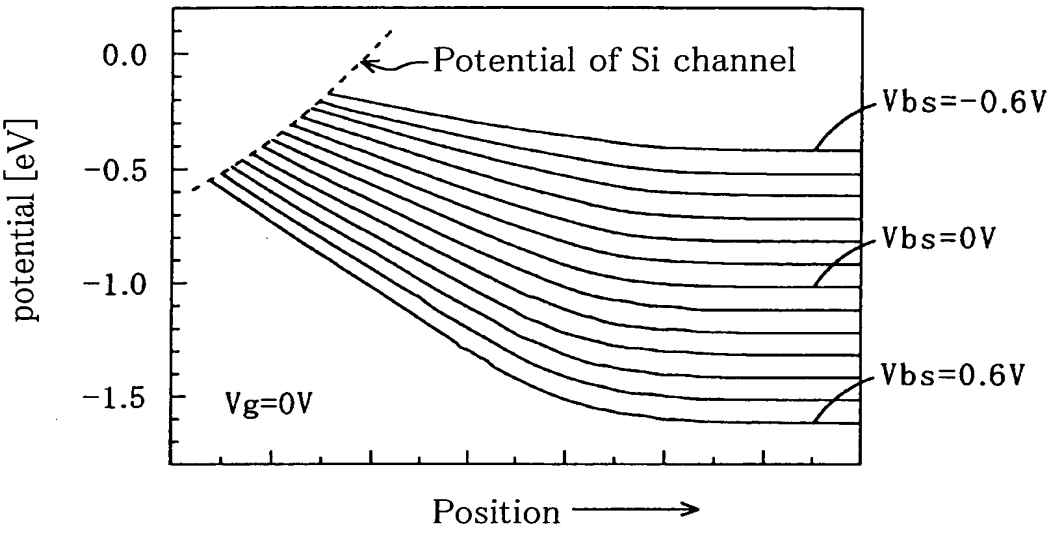

0.0
-0.5
-1.0
-1.5
potential [eV]
Potential of Si channel
Vbs=-0.6V
Vbs=0V
Vbs=0.6V
Vg=0V
Position

Fig. 3(b)

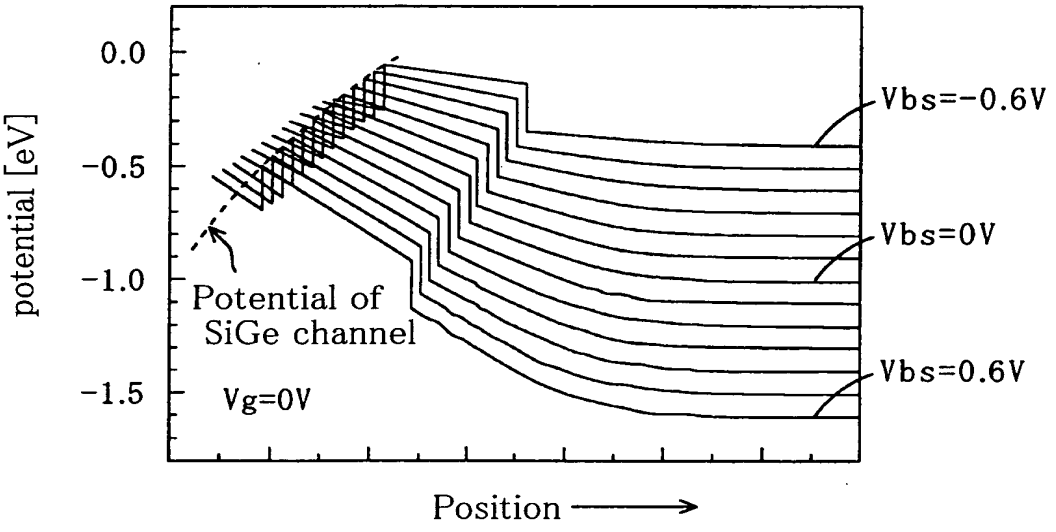

0.0
-0.5
-1.0
-1.5
potential [eV]
Vbs=-0.6V
Vbs=0V
Vbs=0.6V
Potential of
SiGe channel
Vg=0V
Position

Fig. 4

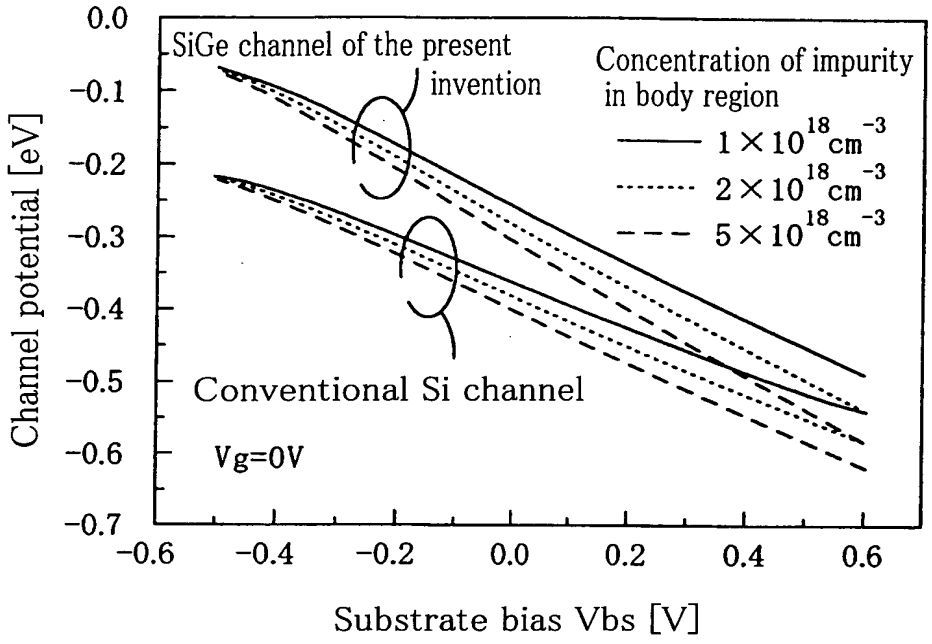

SiGe channel of the present invention
Concentration of impurity in body region
1×10^18 cm^-3
2×10^18 cm^-3
5×10^18 cm^-3
Conventional Si channel
Vg=0V
Channel potential [eV]
Substrate bias Vbs [V]
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
-0.6
-0.7
-0.6
-0.4
-0.2
0.0
0.2
0.4
0.6

Fig. 5

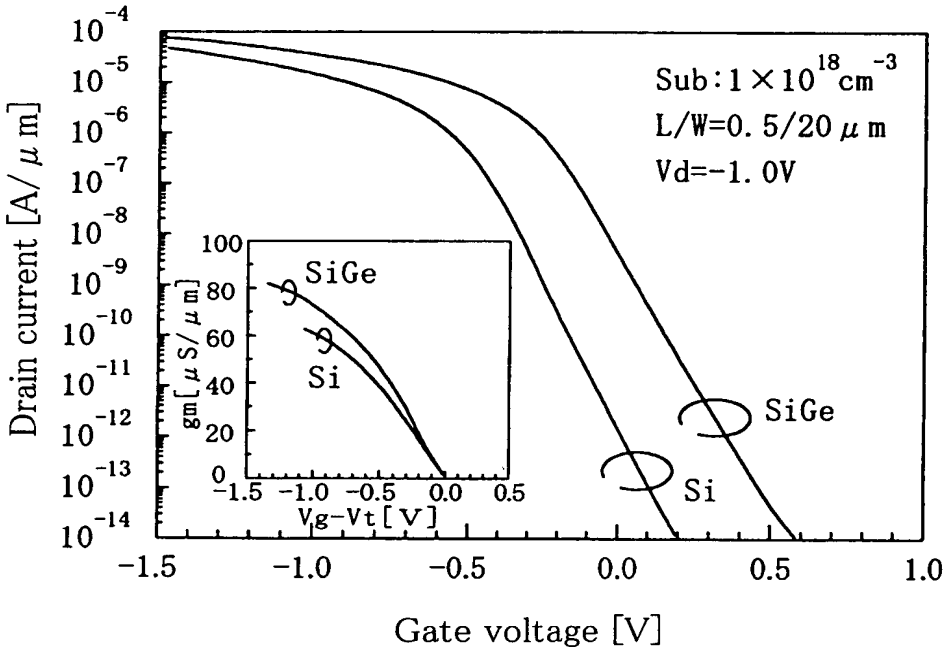

Sub:1×10^18 cm^-3
L/W=0.5/20 μm
Vd=-1.0V
SiGe
Si
gm[μS/μm]
Vg-Vt[V]
Drain current [A/μm]
Gate voltage [V]
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
10^-11
10^-12
10^-13
10^-14
-1.5
-1.0
-0.5
0.0
0.5
1.0

Fig. 6(a)

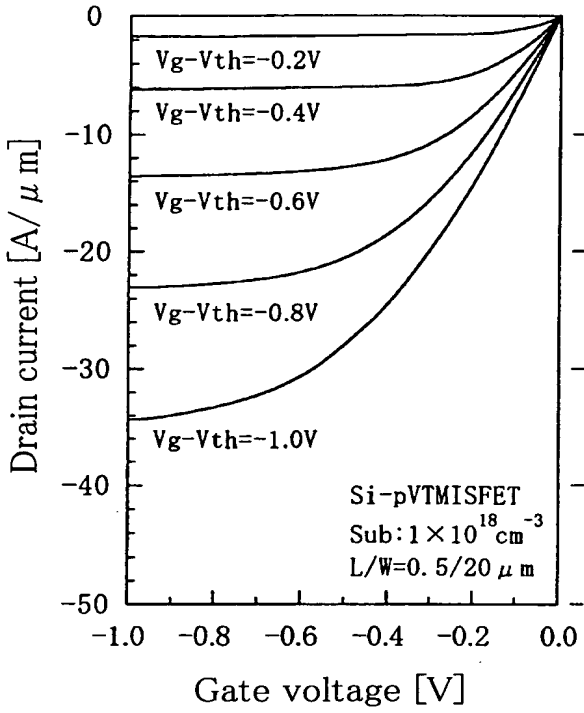

0
-10
-20
-30
-40
-50
Drain current [A/μm]
Vg-Vth=-0.2V
Vg-Vth=-0.4V
Vg-Vth=-0.6V
Vg-Vth=-0.8V
Vg-Vth=-1.0V
Si-pVTMISFET
Sub:1×10^18cm^-3
L/W=0.5/20μm
-1.0
-0.8
-0.6
-0.4
-0.2
0.0
Gate voltage [V]

Fig. 6(b)

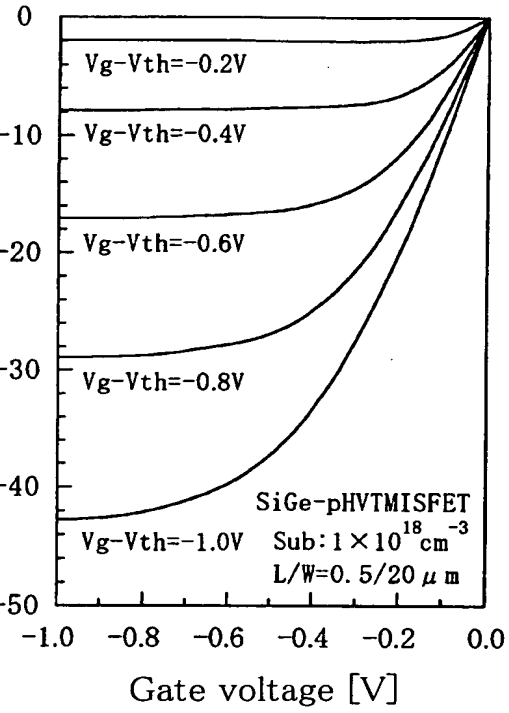

0
-10
-20
-30
-40
-50
Vg-Vth=-0.2V
Vg-Vth=-0.4V
Vg-Vth=-0.6V
Vg-Vth=-0.8V
Vg-Vth=-1.0V
SiGe-pHVTMISFET
Sub:1×10^18cm^-3
L/W=0.5/20μm
-1.0
-0.8
-0.6
-0.4
-0.2
0.0
Gate voltage [V]

Fig. 7

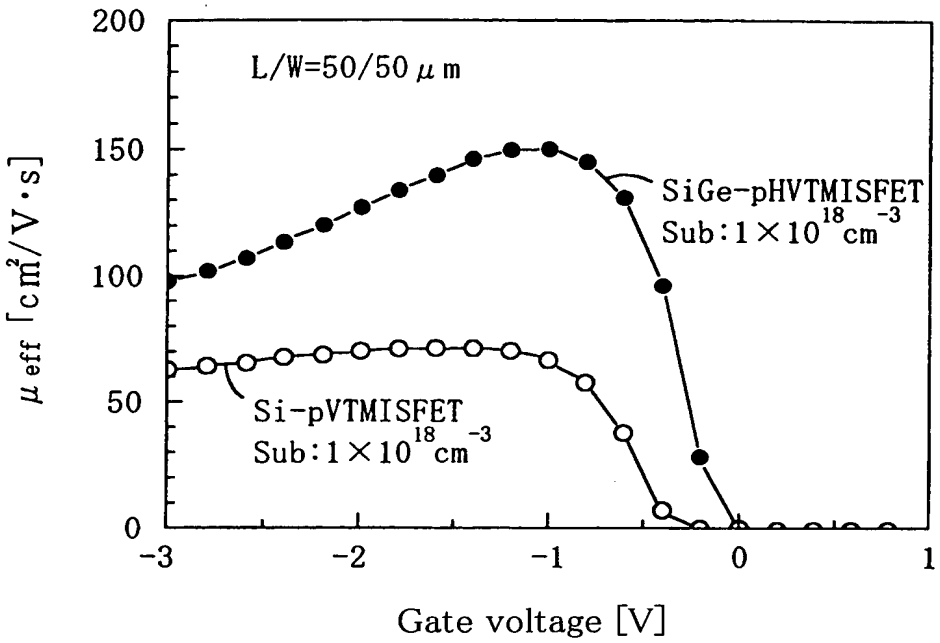

200
150
100
50
0
-3
-2
-1
0
1
L/W=50/50 μm
SiGe-pHVTMISFET
Sub:1×10^18cm^-3
Si-pVTMISFET
Sub:1×10^18cm^-3
μeff [cm²/V·s]
Gate voltage [V]

Fig. 8(a)

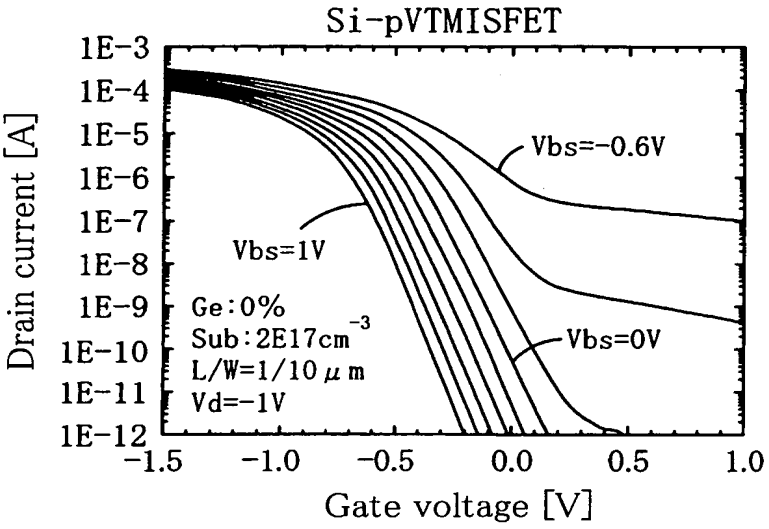

Si-pVTMISFET
Drain current [A]
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
1E-11
1E-12
Vbs=-0.6V
Vbs=1V
Vbs=0V
Ge:0%
Sub:2E17cm-3
L/W=1/10μm
Vd=-1V
-1.5
-1.0
-0.5
0.0
0.5
1.0
Gate voltage [V]

Fig. 8(b)

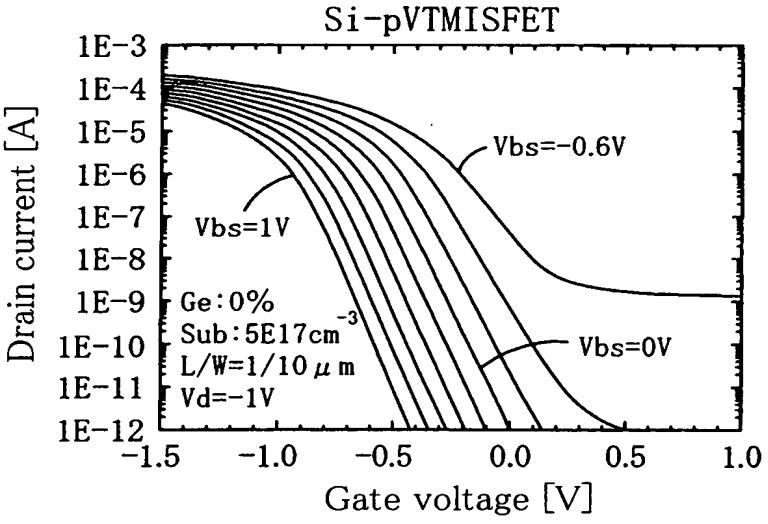

Si-pVTMISFET
Drain current [A]
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
1E-11
1E-12
Vbs=-0.6V
Vbs=1V
Vbs=0V
Ge:0%
Sub:5E17cm-3
L/W=1/10μm
Vd=-1V
-1.5
-1.0
-0.5
0.0
0.5
1.0
Gate voltage [V]

Fig. 9(a)

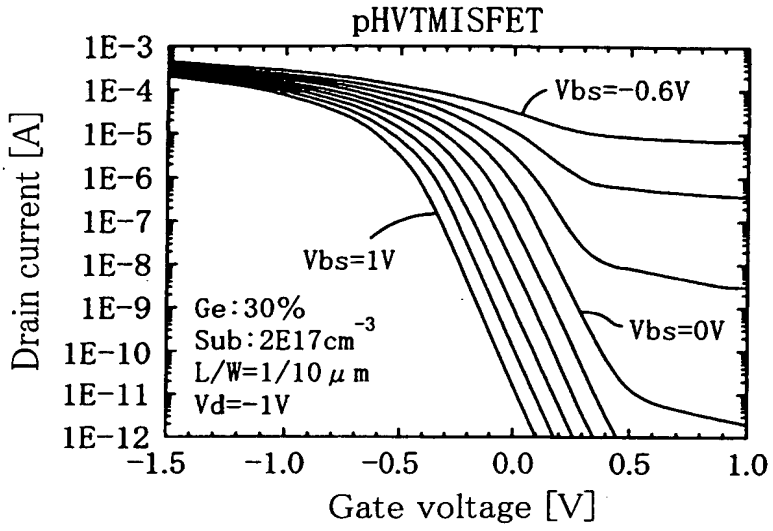


Fig. 9(b)

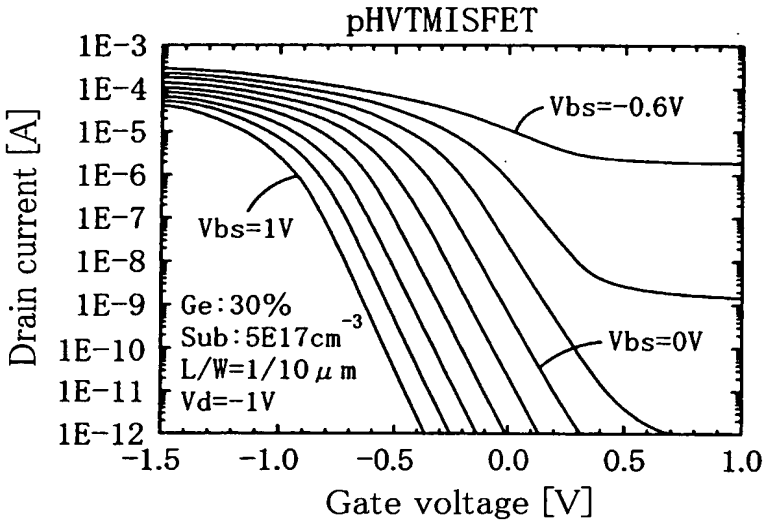


Fig. 9(c)

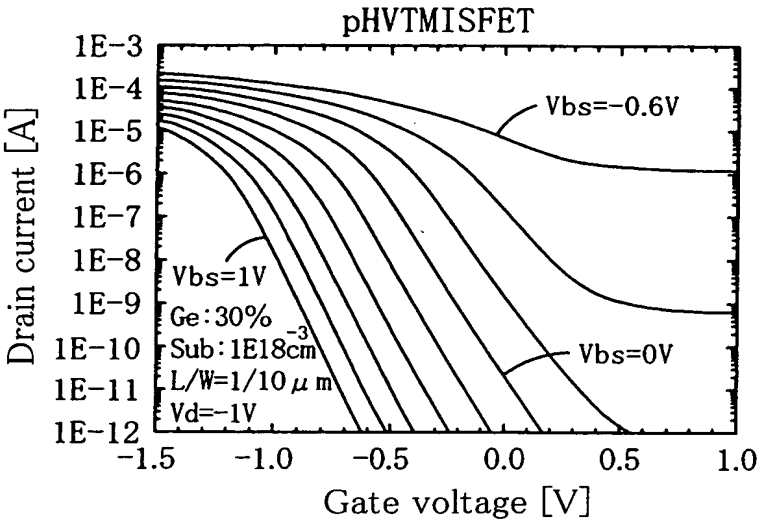


Fig. 10

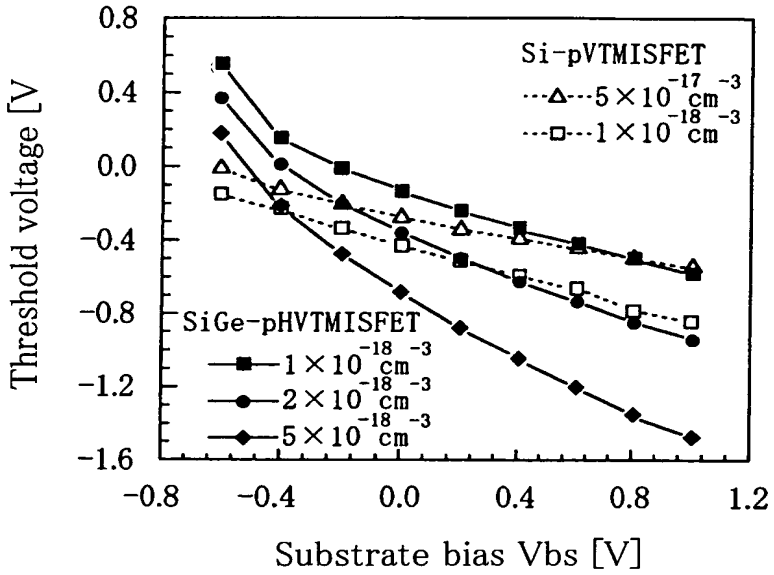

0.8
0.4
0.0
-0.4
-0.8
-1.2
-1.6
-0.8
-0.4
0.0
0.4
0.8
1.2
Threshold voltage [V
Substrate bias Vbs [V]
Si-pVTMISFET
5×10 cm
1×10 cm
SiGe-pHVTMISFET
1×10 cm
2×10 cm
5×10 cm

Fig. 11 (a)

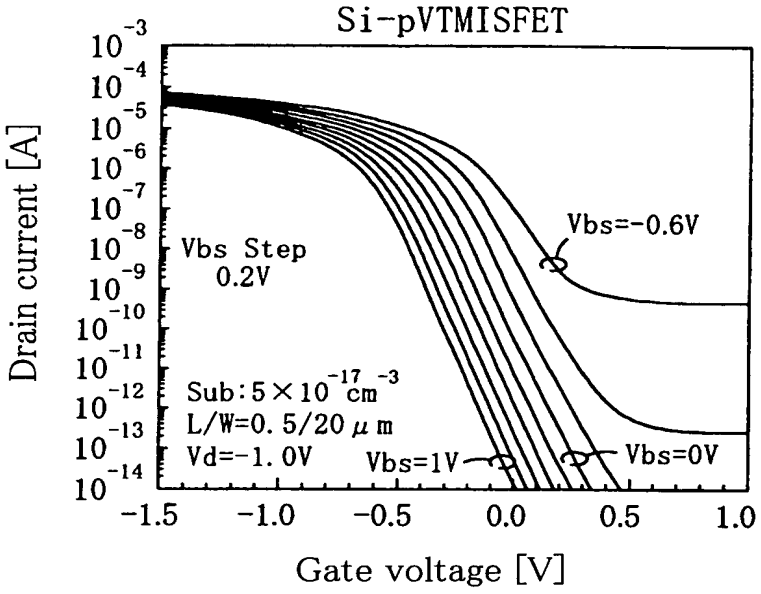


Fig. 11 (b)

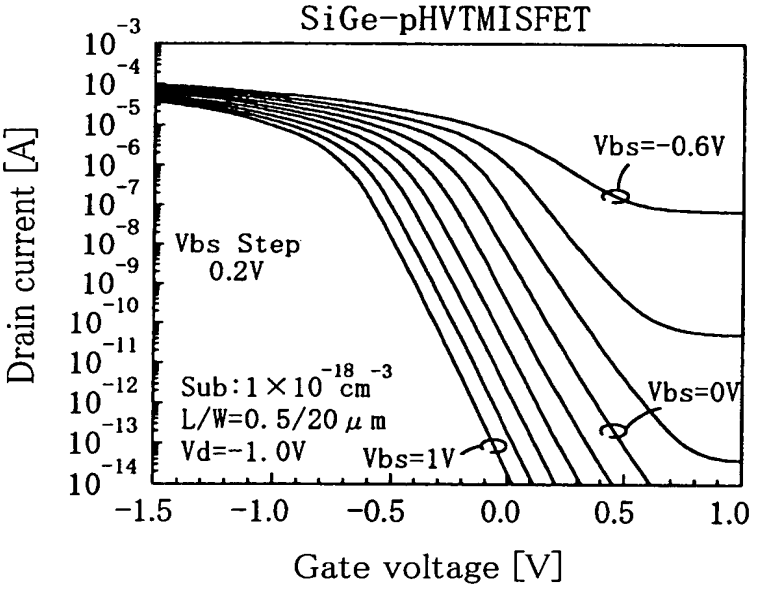


Fig. 12

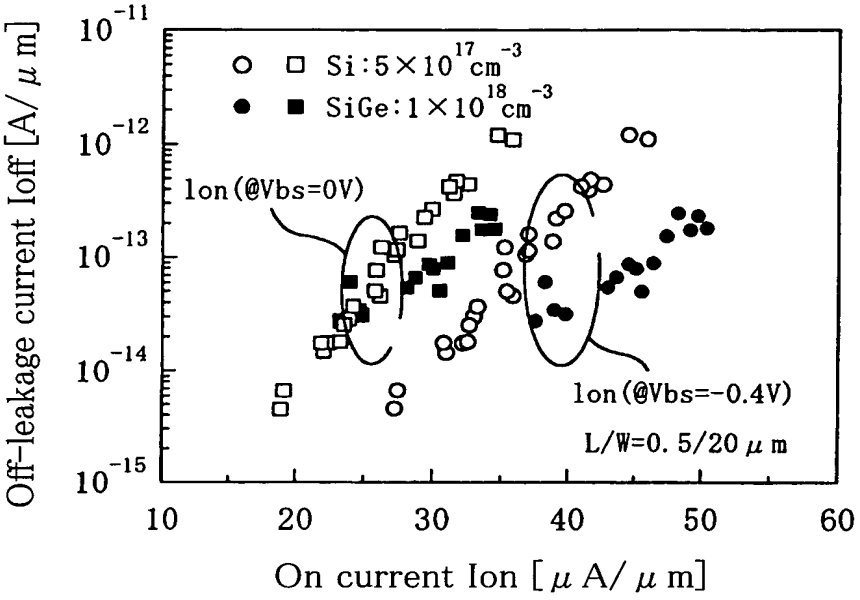

Off-leakage current Ioff [A/μm]
10^-11
10^-12
10^-13
10^-14
10^-15
Si:5×10^17 cm^-3
SiGe:1×10^18 cm^-3
Ion(@Vbs=0V)
Ion(@Vbs=-0.4V)
L/W=0.5/20 μm
10
20
30
40
50
60
On current Ion [μA/μm]

Fig. 13(a)

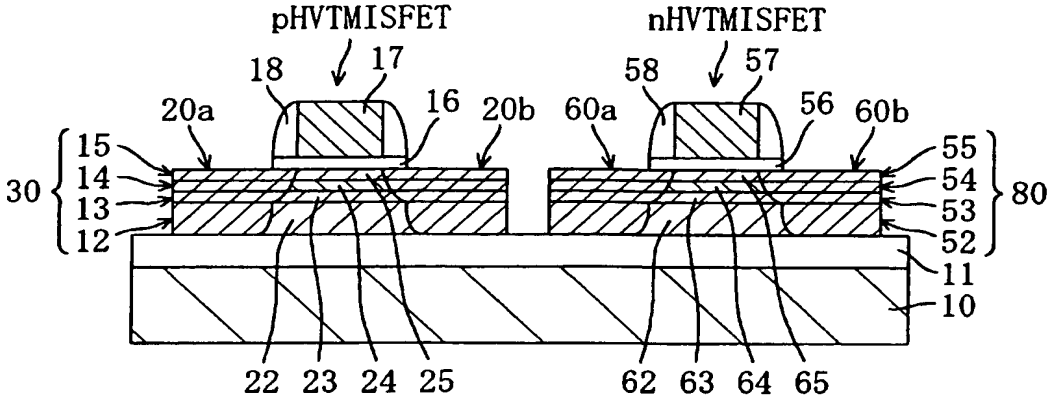


Fig. 13(b)

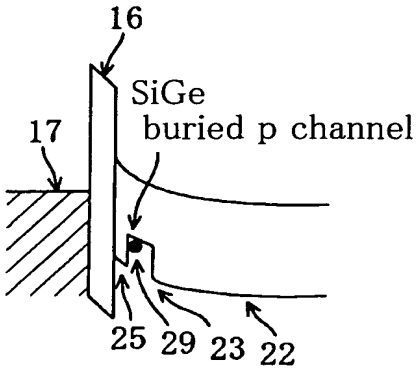


Fig. 13(c)

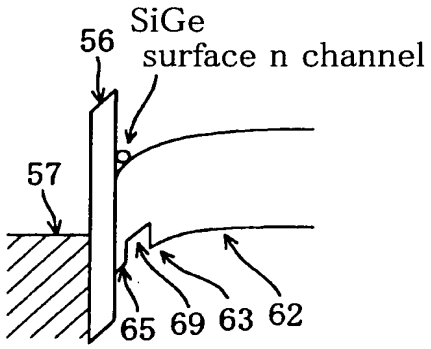


Fig. 14(a)

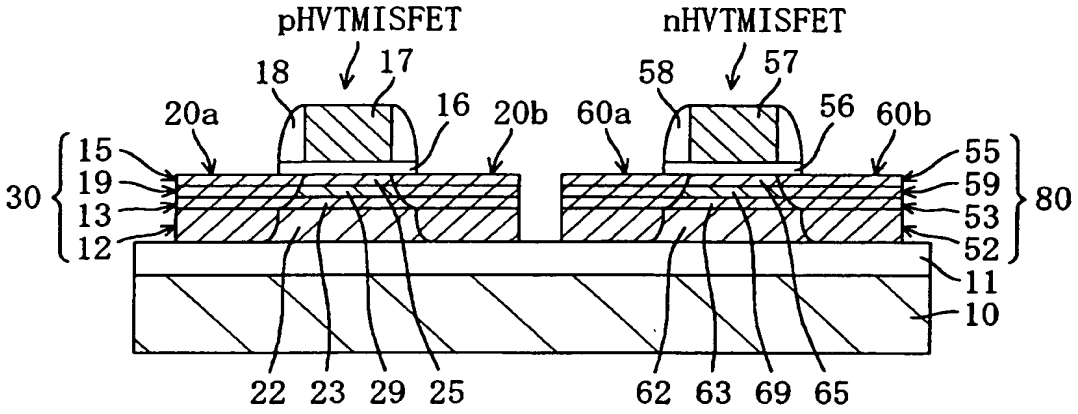


Fig. 14(b)

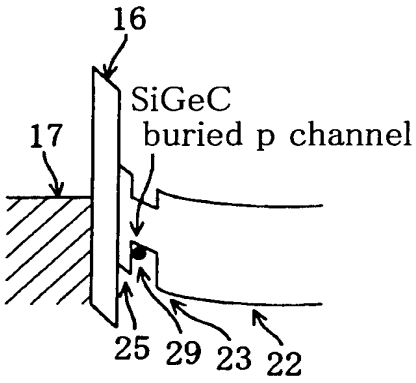


Fig. 14(c)

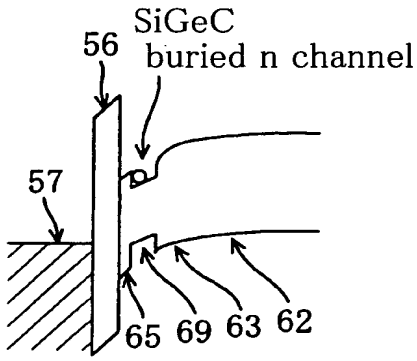
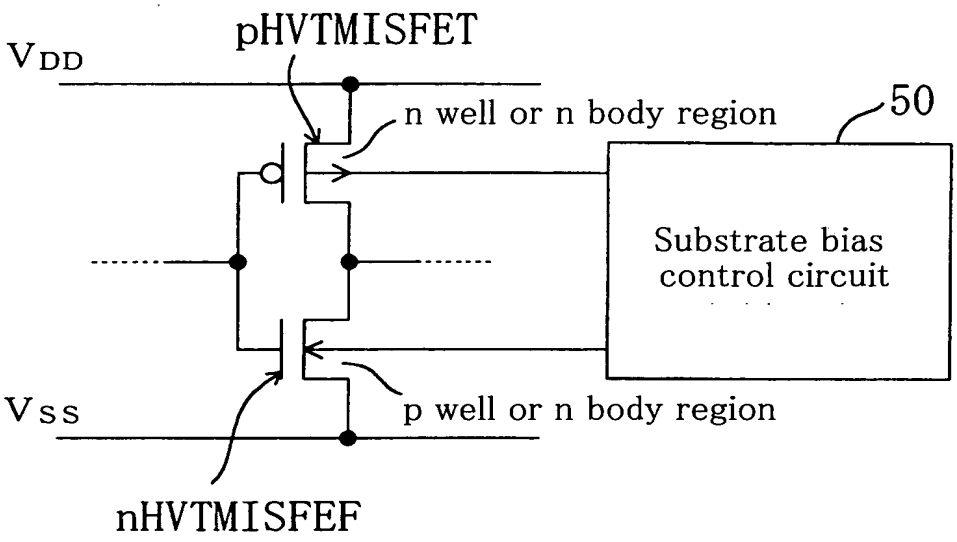


Fig. 15


pHVTMISFET
VDD
n well or n body region
50
Substrate bias
control circuit
Vss
p well or n body region
nHVTMISFEF

[Name of the Document] ABSTRACT

[Abstract]

[Problem] To provide a semiconductor device that may provide both of a high speed operation and a low power consumption.

[Means for Solving the Problem] The HVTMMISFET comprises the Si substrate 10 and the Si buffer layer 13, SiGE film 14, and Si film 15 that are epitaxially grown. Also provided are the high concentration n-type body region 22, the n^-Si region 23, the SiGe channel region 24 including n-type impurity of a low concentration, the low concentration n-type Si cap layer 25, and the body contact 27 for applying a bias to the Si body region 22. By introducing, in the channel layer, a material having a potential to the carrier of the band end in which a carrier runs lower than the potential of a material constituting the body region, the substrate bias coefficient can be maintained to be high while lowering the threshold voltage. Thus, both of the high speed operation and low power consumption can be realized.

[Selected Figure] Figure 1

Patent Applicant History Information

Identification Number [000005821]

1. Date of Modification August 28, 1990
   [Cause of Modification] New registration
   Address: 1006, Oaza-Kadoma, Kadoma-shi, Osaka JAPAN
   Name: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

Number of certification: 2002-3104027